

3 a logic built-in self-test state machine; and
4 a pattern generator capable of generating a scan pattern for use in a state of the logic
5 built-in self-test state machine.

1 19. The integrated circuit device of claim 17, wherein the built-in self-test
2 controller further comprises a memory built-in self-test domain.

1 20. The integrated circuit device of claim 17, wherein testing interface comprises
2 a Joint Test Action Group tap controller.

1 21. A method for performing a built-in self-test on an integrated circuit device,
2 comprising:

3 externally resetting a built-in self-test controller including a logic built-in self-test
4 engine;
5 performing a logic built-in self-test from the built-in self-test controller at a test
6 frequency at least as slow as a slowest frequency of a plurality of timing
7 domains to undergo the logic built-in self-test; and
8 obtaining the results of the performed built-in self-test.

1 22. The method of claim 21, wherein resetting the built-in self-test controller
2 includes initializing a multiple input signature register and a pattern generator.

1 23. The method of claim 21, wherein performing the logic built-in self-test
2 includes:

3 initiating a plurality of components and signals in a logic built-in self-test domain of
4 the dual mode built-in self-test controller upon receipt of a logic built-in self-
5 test run signal;
6 scanning a scan chain upon the initialization of the components and the signals;
7 stepping to a new scan chain; and
8 repeating the previous scanning and stepping until the content of a pattern generator
9 equals a predetermined vector count.

1 24. The method of claim 23, further comprising at least one of:
2 setting a bit in the multiple input signature register indicating an error condition arose;
3 and

4 setting a bit in the multiple input signature register indicating whether the stored
5 results are from a previous logic built-in self-test run.

1 25. The method of claim 21, wherein externally resetting a built-in self-test
2 controller includes resetting a built-in self-test controller including a memory built-in self-test
3 engine and the method further comprises:

4 performing a memory built-in self-test from the built-in self-test controller; and
5 obtaining the results of the performed built-in self-test.

1 26. A method for testing an integrated circuit device, comprising:
2 interfacing the integrated circuit device with a tester;
3 externally resetting a built-in self-test controller including a logic built-in self-test
4 engine;
5 performing a logic built-in self-test from the built-in self-test controller at a test
6 frequency at least as slow as a slowest frequency of a plurality of timing
7 domains to undergo the logic built-in self-test; and
8 obtaining the results of the performed built-in self-test.

1 27. The method of claim 26, wherein resetting the built-in self-test controller
2 includes initializing a multiple input signature register and a pattern generator.

1 28. The method of claim 26, wherein performing the logic built-in self-test
2 includes:

3 initiating a plurality of components and signals in a logic built-in self-test domain of
4 the dual mode built-in self-test controller upon receipt of a logic built-in self-
5 test run signal;
6 scanning a scan chain upon the initialization of the components and the signals;
7 stepping to a new scan chain; and
8 repeating the previous scanning and stepping until the content of a pattern generator
9 equals a predetermined vector count.

1 29. The method of claim 28, further comprising at least one of:
2 setting a bit in the multiple input signature register indicating an error condition arose;
3 and

4 setting a bit in the multiple input signature register indicating whether the stored
5 results are from a previous logic built-in self-test run.

1 30. The method of claim 26, wherein externally resetting a built-in self-test
2 controller includes resetting a built-in self-test controller including a memory built-in self-test
3 engine and the method further comprises:

4 performing a memory built-in self-test from the built-in self-test controller; and
5 obtaining the results of the performed built-in self-test.

1 31. The method of claim 26, wherein obtaining the results includes reading at least
2 one of a logic built-in self-test signature and a memory built-in self-test signature.

1 32. The method of claim 26, wherein interfacing the integrated circuit device with
2 the tester includes employing Joint Test Action Group protocols.